Characterization and monitoring structures for robustness against cyclic thermomechanical stress: design and influence of Ti-Al(Cu) layer scheme

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***Abstract*—A wafer-level test approach based on dedicated test structures sensitive to repetitive-power-pulsing stress is described. The approach is suitable for the qualification of different IC back-end stack options with respect to thermomechanical robustness in an early phase of technology development and for process control purposes. In this work, we investigate low-cycle robustness by end-of-life tests for different smart-power technologies with AlCu backend stack. Compared to reference trials a strong dependence of the mean lifetime on lower metal finger configuration and on the used Ti-Al(Cu) layer scheme is found.**

I. Introduction

During technology development phase and for process control purposes, methods to obtain fast feedback on thermomechanical robustness of the backend stack and thereby a statement of the backend-of-line (BEOL) integrity for integrated circuits (IC) is desirable. In particular, usage of integrated power stages as low-side switches to control inductive loads, e.g. magnetic valves, represents a very harsh application mode for the BEOL in automotive ICs, because of repetitive power pulsing (RPP) operation. Within this operation mode, the power stage has to dissipate the induced power during switch off, leading to a pronounced short increase of local device temperature for each switching cycle (fig. 1) [1]. Repetitive pulsing imposes significant thermomechanical stress on the IC BEOL, which may cause failure of the driver stage [2], [3], [4]. We describe a wafer-level test approach based on dedicated test structures sensitive to RPP stress under highly accelerated monitoring conditions. The method is useful in particular for the qualification of different technology options in an early phase and for process control purposes. Here we focus on usage for fast-feedback qualification tests of variation in structure design and process details. Application for process control monitoring has been discussed elsewhere [5]. First, we summarize test structure design and test approach. For different smart-power BCD technologies we then study the RPP robustness by end-of-life (EoL) tests, first by varying the stress condition for different size and shape of the drivers. In a second step for a suitable RPP reference condition, we investigate the influence of variation of details in a) driver layout, and b) in the Ti-Al(Cu)-layer sequence on RPP robustness.

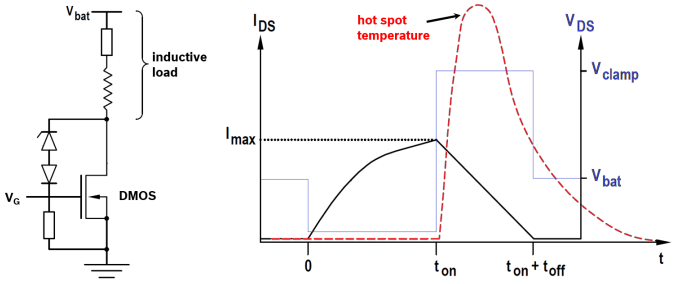

Fig. 1. *Left:* Power stage (DMOS) in clamp induced switching configuration used as low-side switch. *Right:* Schematic of drain voltage (blue line) and current (black line) at the power stage during switching on and off. Due to small gate overdrive of the power stage, a significant self-heating occurs, resulting in a formation of a hot spot in the center of the structure (red-dashed line).

II. Test structure and measurement approach

We derived the test structure scheme from application-near designs of $40\,\mathrm{V}$ and $60\,\mathrm{V}$ nLDMOS output driver stages in Bipolar-CMOS-DMOS (BCD) technology using a planarized AlCu-metal stack with top-Cu power routing. Overall size of the test devices (DUTs) has been chosen between typically $0.5\,\mathrm{mm}^2$ and down to small dimension (side length below $70\,\mu\mathrm{m}$), which can be integrated into scribe line for process control purposes (fig. 2). Further, we implemented comparable structures for different BEOL variants, such that we can investigate RPP robustness influence of BEOL layer scheme and of layout design approach independently. In a typical clamped induced switching configuration, every test structure contains beside the main driver a chain of Zener diodes between drain and gate to limit drain-source voltage V_{DS} and to control gate voltage during power pulse automatically, and a pull-down resistor to draw off gate charge after the power pulse (fig. 3). Optionally the structures also contain up to four tightly embedded NPN-type temperature sensors used to measure transient temperature information locally in the active

978-1-5090-3615-8/17 $31.00 © 2017 IEEE

area during the pulse event [6]. We use an electrothermal simulation approach to analyze local current density, power density and temperature distribution in the metal routing of the power stage. With proper calibration we can thus transfer test conditions to test structures without sensor, e.g. power stages of given products. The simulation uses the electrothermal analyzer ETHAN from Silicon Frontline Technology Inc [7]. It allows a self-consistent transient solution of the current flow in the multi-finger metal stack and power dissipation in the active area of the power stage based on local operation point and temperature. The thermal boundary conditions of the simulator as well as the temperature sensors are calibrated before under well-known test conditions [5].

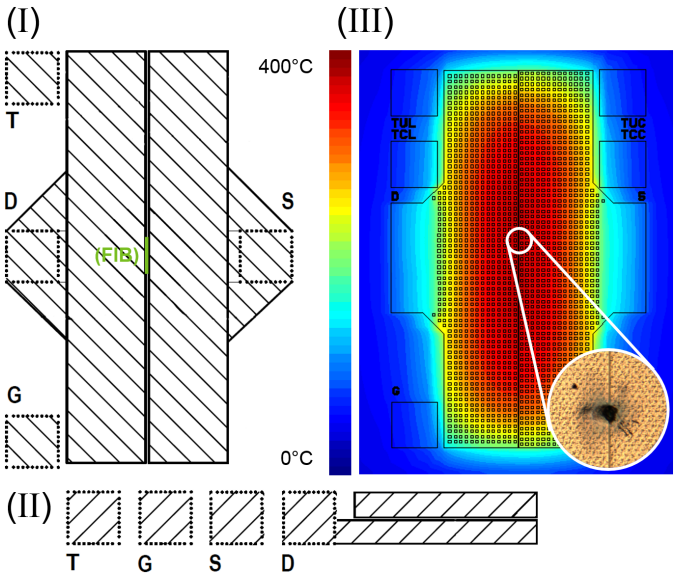

Fig. 2. I, II: Variation of overall device size of the DUT between typically $0.5\,\mathrm{mm}^2$ and small $0.01\,\mathrm{mm}^2$ (top-Cu view). The DUTs contain up to four temperature sensors integrated in the source finger of the device. The line (FIB) indicates the cutting direction during FIB analysis. III: color coded figure indicate the lateral temperature distribution of the device based on an electrothermal simulation at the end of a rectangular power pulse. The inset shows a typical failure location site after RPP EoL test.

Accelerated wafer-level EoL tests are done using a Keithley 2430 1 kW pulsed mode SourceMeter delivering bursts of millisecond rectangular power pulses in an automated setup on a semiautomatic probe station (fig. 3). Typical pulse length is $0.5\,\mathrm{ms}$ with $100\,\mathrm{Hz}$ pulse period. Within the V_{DS}-clamp, the DUT operates at a point of high power dissipation such that each millisecond power pulse leads to a pronounced local temperature excursion in the power stage (fig. 2). A strong lateral temperature gradient imposes severe stress on the IC backend structure due to the mismatch of CTE of aluminum or copper metals and dielectrics, which may cause degradation and IC failure in respective applications [8]. Here we target to operate in the low-cycle lifetime limit for test devices under RPP stress. Much higher pulse energy compared to typical application conditions leads to mechanical stress beyond the yield point of the constituted metals such that each cycle may accumulate a viscoplastic deformation of the metal. Ultimately, stress on dielectrics may exceed critical limits and DUT failure occurs indicated by an electrical detectable leakage path or even short in the source/drain metal path of the driver (see fig. 2). Repetitive pulse stress is applied to the DUT while monitoring V_{DS} leakage in off-state and V_{DS}-value under pulsing. DUT failure is detected by increase of V_{DS} leakage and the system stops pulse stress and steps to the next DUT automatically. Thus, we executed statistical RPP EoL trials and generally modeled the mean RPP lifetime from Weibull analysis by an extended Coffin-Manson approach based on the Norris-Landzberg ansatz [9]. Ambient chuck temperature was $25\,°\mathrm{C}$ in all cases if not stated otherwise.

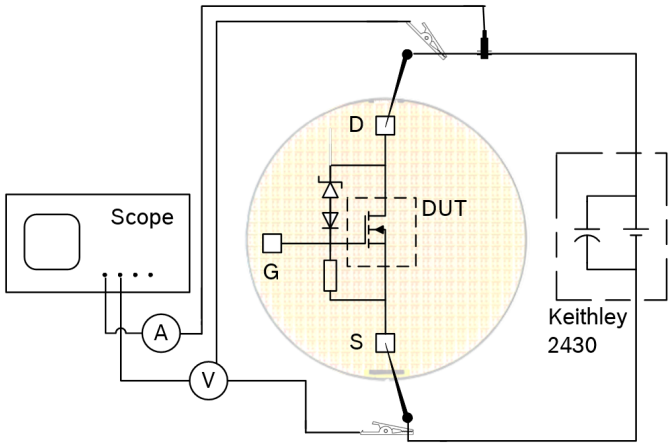

Fig. 3. Schematic of the automated EoL test setup on wafer-level using a semiautomatic probe station. A Keithley 2430 1 kW pulsed mode SourceMeter deliver bursts of millisecond rectangular power pulses. Additionally a scope is used to control drain current, drain-source voltage and temperature sensor readout.

III. RPP LOW-CYCLE LIFETIME RESULTS FOR DIFFERENT SIZE OF STRUCTURE

In first set of trials we studied the influence of design parameters area and aspect ratio on RPP lifetime for a given BEOL scheme 'B' of the given technologies (comp. fig. 7). Stress condition, i.e. pulse energy, has been adopted by means of electrothermal simulation to yield in each case comparable thermal swing ΔT in central hot spot of device. Figure 4 shows the Coffin-Manson plot of mean RPP lifetime vs. thermal swing ΔT of a larger typical and a small DUT, the latter intended for scribe line module (comp. fig. 2). Up to a high thermal swing ΔT of $380\,\mathrm{K}$ per pulse, both trends are well aligned. In general of course area and aspect ratio of the driver significantly influence thermal stress ΔT for given fixed pulse energy (and with it lifetime). Here, however, they do not play a significant role if thermal pulse stress condition is properly considered by means of the electrothermal simulation, i.e. if ΔT is kept constant by adopting the pulse energy for different size and shape. This means that small scribe line structures are well suitable to test or monitor BEOL wear out under fast thermomechanical cycling. For even higher ΔT above $380\,\mathrm{K}$ the larger DUT exhibit a deviation from Coffin-Manson trend to much lower lifetime. In contrary, the small

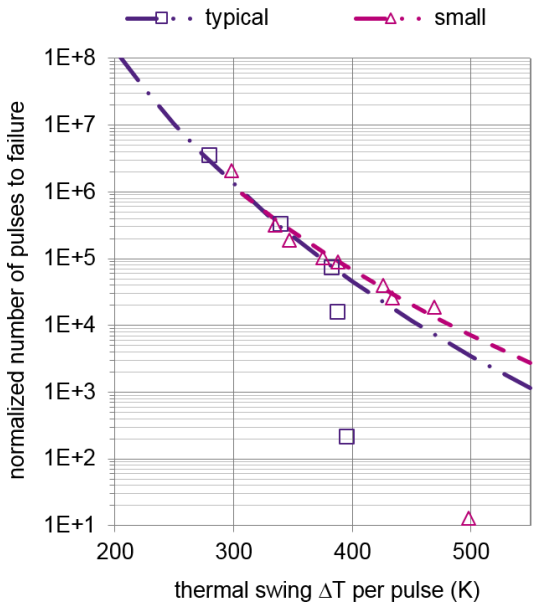

Fig. 4. Coffin-Manson plot of mean RPP lifetime from measured test series (symbols) for different active area of DUT plotted against the thermal swing ΔT based on electrothermal simulations. Dashed and dashed-dotted lines indicate fitted Coffin-Manson-trend.

area devices can be stressed up to peak temperature above $500\,\mathrm{K}$ without early failures, i.e. close to the limitation of the electrothermal save operating area of the used nLDMOS devices [5].

As a possible reason for the lower lifetime of the larger DUTs close to $\Delta T = 380\,\mathrm{K}$ and above we considered electromigration (EM) as additional failure mode. Based on the results of ETHAN simulation, we determine a maximum current density of $3\,{}^{\mathrm{mA}}/_{\mu\mathrm{m}^2}$ in the third AlCu metal level for the corresponding power pulse leading to a thermal swing of approximately $400\,\mathrm{K}$. These metal shapes with maximum peak current density distribute the current to regions of the power stage, which are not directly connected to source or drain upper copper plate. Assessment of the corresponding EM stress based on the standard model following Black´s equation with conservative parameters yields a number of pulses to failure of about $8.2E+06$ assuming a quasi-dc stress condition. This leaves much headroom compared to our results and thus cannot explain the drop in the RPP lifetime of the larger DUTs. The reason for the short lifetimes of the larger DUTs at high ΔT (and with it high peak temperature) is still under investigation. However, the corresponding failure mode is typically not relevant for the application under discussion. In the following studies comparing different design and BEOL options stress experiments have operated below the $380\,\mathrm{K}$ limit.

IV. Routing Scheme vs Device Lifetime

To evaluate the influence of routing scheme on device lifetime of the given technology option 'B' (comp. fig. 7) and to test the method regarding fast feedback of different design variants of the power stage, we carried out a further set of trials. Thereby the detailed metal layout of the test structures has been varied within design rules margin, which can be seen in figure 5. For a correct connection of the source and drain active areas of the power stage, the pitch of lower AlCu metal levels was kept constant and the distance between the metal fingers was varied. This results in a varied ratio of the lateral interlayer dielectric (ILD) to metal filling proportion in the complete stack of lower metal levels. By the different metal finger spacing, this filling ratio changes from $48\,\%$ to $7\,\%$. These values represent the maximal proportion of ILD, where the pitch can be hold constant in terms of sufficient via overlap during process flow, and the minimal proportion with respect to technology design rules. Additionally to avoid a high current density in the zone between the upper copper plates, where current is partially distributed further by lower aluminum lines, for this test series a different layout is used. Compared to figure 2, the top copper layer is designed as finger structure. To increase the finger width, the lower aluminum lines are rotated by 90°, so that the copper level is independent of lower aluminum pitch.

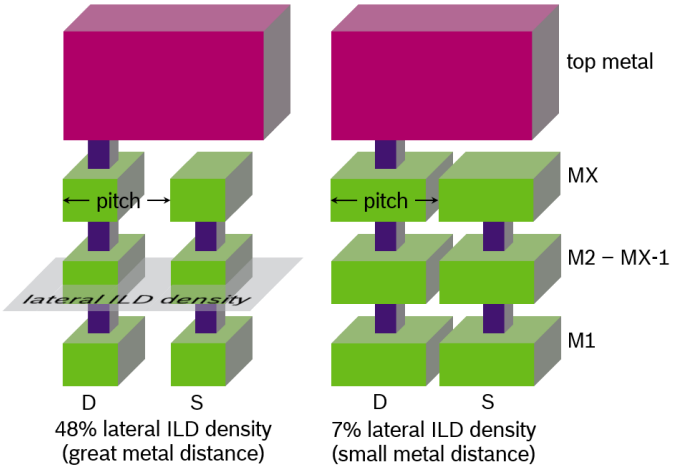

Fig. 5. Schematic of the aluminum finger configuration in the lower metal levels. The lateral ILD density is varied between $48\,\%$ and $7\,\%$ at constant pitch.

While area and aspect ratio has negligible influence on RPP wear out, a significant dependence of RPP lifetime on the chosen layout configuration is seen (comp. fig. 5): The higher dielectric proportion present in lower-metal layer stack yields up to tenfold higher thermomechanical robustness in terms of RPP EoL (fig. 6). While Weibull slopes drops from 16.8 to 2.6, for the wide metal structures, i.e. low ILD filling ratio, the larger aluminum volume generates a higher amount of mechanical stress on the dielectric during expansion because of lateral thermal gradient in the metallization stack. Additionally thermomechanical simulations show a reduced overall stiffness leading to a pronounced strain under RPP [10].

Faster (intrinsic) RPP wear out by worst-case layout approach may be desirable for process assessment and monitor-

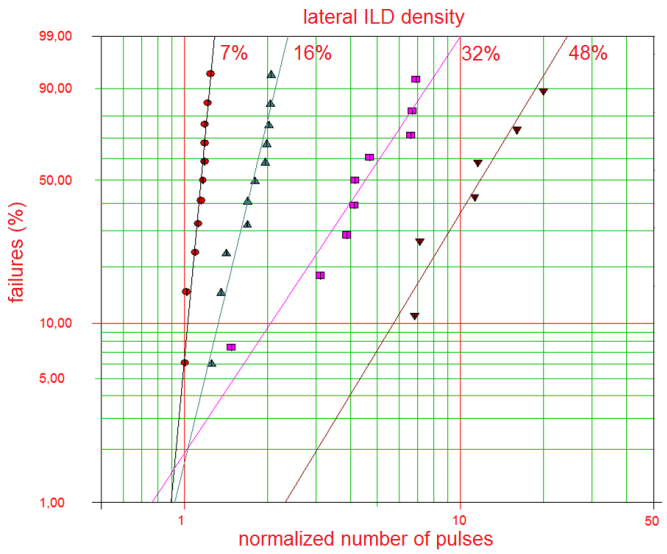

Fig. 6. Lifetime distribution of a set of trials with varied lower metal layout scheme. The structures with higher lateral ILD density in the metal stack have a longer mean lifetime of about one order of magnitude.

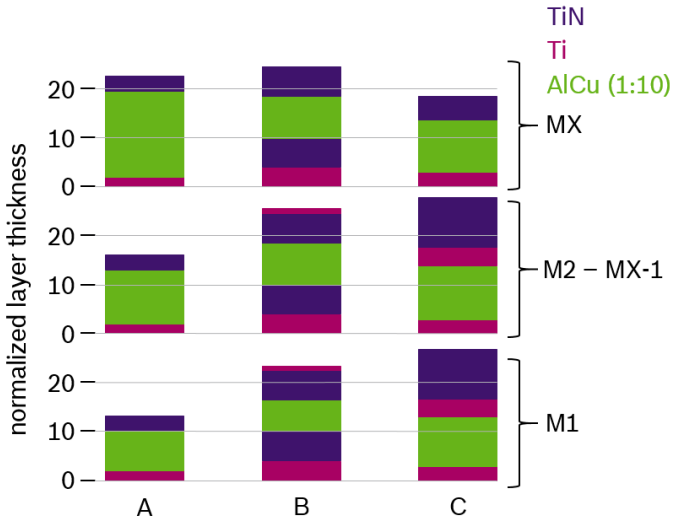

Fig. 7. Schematic comparison of material layer sequences before annealing for the metal levels M1 - MX (uppermost thin metal level) of the investigated BEOL configurations. Variant 'A' is produced with a relatively thick uppermost aluminum layer to improve power distribution in this metal level. Variant 'B' show relatively small aluminum thicknesses for all metal levels which increase thermomechanical robustness with respect to RPP. Variant 'C' is related to Variant 'B' but compensates electromigration issues of the Al-lines by embedding them in a Ti-coat which results in a formation of $TiAl_3$.

ing purpose. Area-efficient application design, on the contrary, needs highest intrinsic RPP stability, which is obtained using a higher dielectric proportion. However, design for application has to fulfill requirements in terms of peak current density in the metals and on-state resistance $R_{DS(on)}$ of the drivers, too. The lower-metal aluminum fingers have to ensure electrical connection between the upper copper fingers and the active area of the power stage. Here the maximum current density increases for increased lateral ILD density: Regarding the total current used in the RPP trial for ILD density $7\,\%$ current density is $0.486\,{}^{\mathrm{mA}}/_{\mu\mathrm{m}}$ and for ILD density $48\,\%$ it is $0.505\,{}^{\mathrm{mA}}/_{\mu\mathrm{m}}$, respectively. These density values are still well below limits to be considered for EM reliability and for self-heating reasons for the given technology. So again, we exclude an influence of EM on these RPP EoL results for the different designs of metal routing. Generally, the used layout design approach leaves enough headroom to fulfill the EM reliability requirements for a robust device under harsh environmental conditions. Regarding $R_{DS(on)}$ the impact of smaller lower-metal fingers is layout dependent. For our layout scheme, we see only a small increase of $R_{DS(on)}$ from $230\,\mathrm{m\Omega}$ to $231\,\mathrm{m\Omega}$ for the increase in lateral ILD filling ratio. This deterioration is lower than $1\,\%$ and practically can be neglected. Regarding electrical connection of power stages with a design based on higher lateral ILD filling, we thus can get a significant improvement of the backend robustness against RPP, while the main electrical parameters remain practically unchanged.

V. Influence of Backend Layer Scheme

In a further analysis we applied the accelerated test approach to compare the influence of Ti-Al(Cu) layer scheme in the BEOL stack (fig. 7). Compared to the reference stack 'B' discussed so far, in a first variant 'A' prominently the uppermost AlCu metal layer thickness has been increased. Further for stack 'B', to improve process stability and adhesion between the applied layers, additional Ti and TiN-layers were implemented. AlCu yield stress increases for decreasing thin film thickness and previous results indicate improved RPP robustness with decreasing film thickness [8]. For comparison of the different BEOL variants we determine the thermal swing needed to reach EoL for a fixed reference lifetime condition, see figure 8. As shown compared to 'B', variant 'A' exhibits a significantly lower stress level of about -150K per pulse for same RPP lifetime. Thus within stack 'B' with reduced AlCu film thickness overall thermomechanical robustness is strongly enhanced and allows area optimization of respective driver stages in the IC designs. Thinner AlCu layers exhibit increased current density levels for similar target currents. Focused on the compensation of the increased EM vulnerability in the metal levels of variant 'B', a further variant 'C' is investigated by directly embedding the aluminum lines in thicker bottom and top Ti-layers. After an annealing step during process flow, this configuration results in the formation of a $TiAl_3$-coat, whereby the thickness of the overall stack of the metal level is reduced slightly. This Ti/TiN layer approach is known to enhance EM robustness [11], [12]. For RPP, however, compared to the previous results of variant 'B', this configuration 'C' gives a significant lower robustness of about -100K per pulse for the same lifetime level (fig. 8). This trend of different RPP robustness between 'A', 'B' and 'C' is confirmed for different stress levels although respective Coffin-Manson parameters differ slightly.

For root-cause analysis of the observed lower robustness of variant 'C', we prepared a set of DUTs at different lifetime

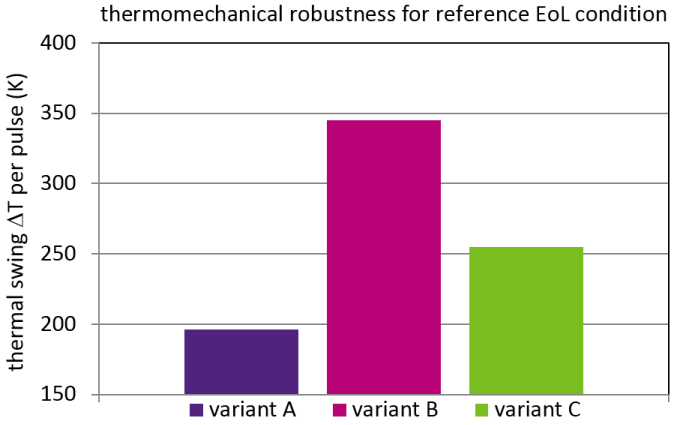

Fig. 8. Minimal amount of thermal swing ΔT per pulse which is necessary to destroy the power stage due to repetitive power pulsing within a reference EoL condition. The largest thermomechanical robustness can be observed for variant 'B'.

states for cross-section analysis with the help of a focus ion beam (FIB) system. Based on the known mean number of pulses for EoL from the steep Weibull distribution (slope 5.5), DUTs have been stressed and stopped at different nominal lifetime states. The cross sections are recorded using secondary electron detection with a magnification of 30 000. The cutting direction of the cross sections lies between the upper drain and source copper plate and is shown in figure 2. Thereby the degradation under stress of the upper part of the aluminum stack is in focus, where the greatest thermomechanical stress is expected [3], [10]. Image 9 (I) shows the metal levels of a fresh device, which is not stressed by RPP. The metal lines indicate the grains of $TiAl_3$ formation, formed due to an annealing step, which is done after every metal level deposition. Because of a single Ti-Layer at the bottom of the upper aluminum layer, this metal line show the $TiAl_3$ grains only at the lower surface. The grains extend up to $200\,\mathrm{nm}$ and protrude clearly into the metal layer due to the aluminum consummation during formation, which is responsible for a slightly decreasing metal level thickness.

After bursts of $52.8\,\mathrm{W}$ power pulses, the second image 9 (II) shows the same cross section for a DUT with a lifetime progress of $50\,\%$. It can be determined that $TiAl_3$ grains become smaller and can drift through the aluminum. As mentioned before applying RPP for the given BEOL variation results ultimately in the occurrence of a leakage path between source and drain leading to the destruction of the power stage. To complete the evolution series, we prepared also one DUT, which is stressed until a leakage path can be measured. The cross section of this device is shown in figure 9 (III) and does not correspond to the failure site, however. Here the FIB cut additionally shows a formation of voids. This region has a particularly high current density because of the current distribution in areas of the power stage, which are not directly connected to an upper copper plate. Therefore, the aluminum fingers are more vulnerable for EM effects. Another mechanism which leads to the formation of voids, can be stress induced voiding based on thermomechanical gradients [13], [14], [4]. They can be build up during process flow or are a result of RPP stress. To investigate the origin of voiding more analysis based on stressed metal stacks without current flow are necessary to avoid the influence of EM completely. Furthermore, figure 9 (III) shows $TiAl_3$ grains orientated vertical, connecting the top and bottom $TiAl_3$-coat of the metal level. This effect can have a pronounced influence on the sheet resistance, which is already seen in literature [15]. If this effect is also primarily caused by repetitive mechanical stress gradients or if it is a result of the electron wind, has to be clarified by further analysis.

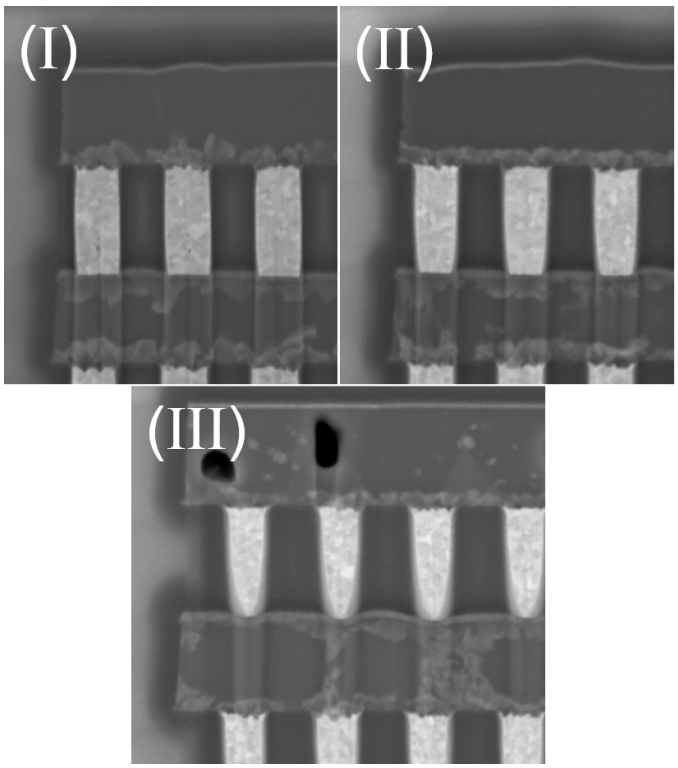

Fig. 9. Cross sections of the upper part of the aluminum stack of three DUTs after stress trials corresponding to $0\,\%$ (I), $50\,\%$ (II) and $100\,\%$ (III) lifetime. The DUTs are prepared under highly accelerated stress conditions with burst of $52.8\,\mathrm{W}$ for $0.5\,\mathrm{ms}$ power pulses. The analysis is based on secondary electron detection with a magnification of 30 000. The cutting direction of the cross sections during FIB analysis is shown in figure 2.

VI. Conclusions

Our results show that very valuable feedback on thermomechanical BEOL robustness of IC technology can be obtained by usage of dedicated test structure approach and wafer-level testing. The approach is suitable for the qualification of different IC backend stack options with respect to thermomechanical robustness in an early phase of technology development and for process control purposes. For different smart-power BCD technologies with AlCu BEOL stack we investigated the low-cycle robustness limit by end-of-life tests for different size and aspect ratios of drivers. From this analysis reference conditions have been derived allowing fast tests with as high thermal

swing per pulse as possible while staying in the normal Coffin-Manson lifetime trend of the RPP degradation. Using these test conditions in comparative trials it has been found that mean RPP lifetime of the driver structures is enhanced when using higher ILD filling ratio in lower metal level stack. Additionally the effect of the detailed barrier layer scheme in the Ti-Al(Cu) metal stack has been investigated. Here the approach without barriers allowing reaction of Al with Ti gave a detrimental effect on the RPP robustness.

ACKNOWLEDGMENT

Part of this work has been conducted in the project eRamp (grant agreement N°621270), co-funded by grants from Austria, Germany, Slovakia and the ENIAC Joint Undertaking. We thank our colleagues Hans-Helmut Kuge, Christian Maier and Franz Dietz for helpful discussions. Also we would like to thank Marcus Schill and Mathias Knaier for FIB support.

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